

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently amended) A delay locked loop comprising a line of n delay cells (R1, R2, ..., Rn) mounted in series; ~~from a delay signal output by the loop being output from the output of one of the delay cells, the input of the delay cells line being connected to a first input of a phase/frequency detector (1), for which a second input is connected to an output from the delay cell, characterised in that the loop comprises control means (4, 7) capable of modifying the output from the delay cell connected to the second input of the phase/frequency detector (1), at the rate of a clock signal (H) when stimulated by control information (I).~~ cell of rank 1 to a delay cell of rank n, n being an integer greater than or equal to 2, each delay cell outputting a delayed signal, the line of delay cells having an input which is an input of the delay cell of rank 1 and which is connected to a first input of a phase/frequency detector, wherein said delay locked loop comprises control means having n inputs and an output, each input of the control means being connected to an output of a different delay cell of the line of delay cells and the output of the control means being connected to a second input of said phase/frequency detector, said control means selecting at each clock signal (H), on the basis of a control information (I), which delayed signal among the different delayed signals is applied to said second input of said phase/frequency detector.

2. (Currently amended) Delay locked loop according to claim 1, ~~characterised in that~~ wherein the control means comprise multiplexing means (4) with n inputs and one output, each ~~input of the multiplexing means (4) being connected to one different delay cell output, the output from the multiplexing means being connected to the second input of the phase/frequency detector.~~

3. (Currently amended) Phased locked loop according to claim 2, ~~characterised in that~~ wherein the multiplexing means (4) comprise a multiplexer (5) and a sigma delta modulator (6) with a clock input on which said clock signal (H) is applied and a signal input on which said control information (I) is applied, the sigma delta modulator (6) outputting a digital control signal applied to the multiplexer (5).

4. (Currently amended) Delay locked loop according to claim 1, ~~characterised in that~~ wherein the control means comprise a first set of n switches I_{qi} ($i = 1, 2, \dots, n$), a second set of n switches I_{pi} ($i = 1, 2, \dots, n$) and a control circuit (7) with a clock input on which said clock signal (H) is applied and a control input on which said control information (I) is applied, the switch I_{pi} ($i=1, 2, \dots, n$) being placed at the output from the ~~rank-i~~ delay cell R_i of rank I ($i=1, 2, \dots, n$) and the switch I_{qi} being placed in parallel with ~~the an~~ assembly formed by the ~~rank-i~~ delay cell R_i of rank i and the switch I_{pi} , switches I_{pi} and I_{qi} being controlled by control signals p_i and q_i respectively output from the control circuit (7).

5. (Currently amended) Delay locked loop according to claim 4, ~~characterised in that~~ wherein additional switches and switchable loads are placed at the input and output of the different delay cells (R_1, R_2, \dots, R_n) such that the total number of switches used in the loop during operation of the loop is always the same, and each delay cell always sees the same load on its input and on its output.

6. (Cancelled)

7. (Currently amended) Delay locked loop according to claim 1, ~~characterised in that~~ wherein the control information (I) is a fractional value p/q such that the output from the delay line is composed of the output from the rank $n-1$ delay ~~line~~ cell for ~~p clock~~ p ticks of the clock signal and the output from the rank n delay ~~line~~ cell during ~~q clock~~ q ticks of the clock signal, where p and q are two integer numbers and q is greater than p , and the value of the delay of a delay cell is given by the relation:

$$\Delta t = q T / (qn - p),$$

where T is the period of a signal applied to the input of the delay line.

8. (Currently amended) Delay locked loop according to claim 1, ~~characterised in that~~ wherein the clock signal (H) is ~~identical a same signal to~~ as a clock signal applied to the first input of the phase/frequency detector (1), except for a delay.

9. (Currently amended) Delay locked loop according to claim 1, ~~characterised in that~~ wherein the clock signal (H) is a signal with a period less than the period of ~~the~~ a signal applied to the first input of the phase/frequency detector (1).

10. (Currently amended) Delay locked loop according to claim 1, ~~characterised in that~~ wherein it comprises means (8, 9, 10) to select a number of delay cells such that the loop will not get locked, during a loop latching phase.

11. (Currently amended) Delay locked loop according to claim 10, ~~characterised in that~~ wherein the means (8, 9, 10) provided to select ~~the~~ a number of delay cells to prevent the loop from getting locked, during a loop latching phase, comprise a convergence analysis device (8), a switch (9) and a processing circuit (10), the input to the convergence analysis device (8) being connected to the output from the phase/frequency detector (1), the switch (9) being controlled such that the output from the convergence device (8) is connected to the input to the processing circuit (10), the output from the processing circuit (10) being connected to a control input of the control means (4, 7).

12. (Previously presented) Delay locked loop according to claim 10, characterised in that it comprises means (10) of memorising the selected number of delay cells.